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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,436	12/03/2003	Kenji Nemoto	04208.0196	5335

7590 03/09/2005

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,436	NEMOTO, KENJI	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003 and 01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04012004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "P1" and "P2" have been used to designate both a current source P1,P2 controlled by the output of differential amplifier OP1 (i.e. see Fig. 6) and a current mirror P1,P2 within a differential amplifier (i.e. see Fig. 2). "NP21" is shown as a base-emitter connected PNP transistor in Fig. 3, and as a base-collector connected NPN transistor within Fig. 6. PN11–PN1n of Fig. 3 do not correspond to PN11-PN1n of Fig. 5. For example, PN11 of Fig. 3 is a base-emitter connected transistor, and PN11 of Fig. 5 is a base-collector connected transistor. PN12 and PN1n of Fig 3 are both diode connected NPN transistors, wherein PN12 and PN1n of Fig 5 are PNP transistors, and they are not diode connected. Therefore, corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are also objected to because some reference designators and connections within Fig. 3 are believed to be incorrect. For example, if Fig. 3 supposedly comprises only NPN transistors, why are PN11 and NP21 both shown as PNP transistors? Also, the bases of those two transistors are believed to be connected incorrectly. A diode connected bipolar transistor typically has its base coupled to its collector, not a base to emitter connection. If the applicant believes Fig. 3 is shown correctly, a detailed description of its operation is requested, especially with respect to PN11 and NP21. The labeling of transistors PN11–PN1n in Fig. 3 is believed to be incorrect. Shouldn't they be identified as NP11, NP12, and NP1n to correspond with how the other NPN transistors within Figs. 2, 3, and 6 are shown/labeled? Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The applicant is reminded of the proper content of an abstract of the disclosure.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art. In this case, it is suggested the sentence "This eliminates...as required in the prior art." be reworded, or at least the phrase "as required in the prior art" be deleted.

The language of the abstract should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc. For example, "the present invention" cited on the first and thirteenth line of the abstract is not necessary. One of ordinary skill in the art would already understand the abstract should be describing the claimed invention.

The abstract of the disclosure is objected to because the terms within the equations are not clearly identified. For example, what does "VBE1n" actually refer to? Also, what does "n" itself refer to (e.g. an integer or constant)? Corrections and/or clarifications are required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: The description on lines 6-9 of page 3 is misleading because it is not understood how the NPN transistors are connected to the input terminals "via diodes." Using the applicant's own Prior Art Fig. 6 as an example, where are the diodes between NP1n and OP1, and between NP2n and OP1? Page 3, line 13 "the both" should be --both-- to improve word flow. Page 5, lines 7-8 "each having a larger emitter area than the first bipolar transistor" needs clarification. For example, if the first bipolar transistors can be of different areas, which one would be considered "the first bipolar

transistor", or does "than the first bipolar transistor" actually mean --than each of the first bipolar transistors--? The following sections also have the same larger area type problem as described above: page 5, line 27 – page 6, line 1; and on pages 6 (lines 23-24); 8 (line 7); 9 (line 13); 10 (line 21); 14 (line 13); and 17 (line 6). Page 9, line 14 "an collector" should be --a collector--. It is believed "corresponding power source" on line 26 of page 9 should actually be --corresponding current source--. Otherwise, "power source" needs to be clarified. Appropriate corrections and/or clarifications are required.

Claim Objections

Claims 4-7, and 9-10, are objected to because of the following informalities: Other than the use of "a" versus "an", lines 11-12 and 13-15 of claim 4 both recite "a(n) collector of each of the group of second pnp transistors being grounded,". Therefore, it is suggested the "an collector... being grounded," on lines 11-12 be deleted to remove the redundant type phrase. Claim 5, line 20 "n-th the group" should be --n-th of the group-- to improve word flow. Claims 6 and 9 carry over the objection from claim 4 when they depend on that claim. Claim 7, line 11 "an" should be --a-- to improve word flow. It is suggested "a" be deleted from line 11 of claim 9 to improve word flow, and to correspond to its "first and second input terminals" phrase. Similar to claim 9 (line 11) above, it is suggested "a" be deleted from line 7 of claim 10, and from line 12 of claim 11, to correspond to its "first and second input terminals" phrase. Claim 11, lines 24 and 34 should have --transistors-- instead of "transistor" to ensure consistent labeling throughout the claim. Dependent claims carry over any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The phrase "a larger emitter area than the first bipolar transistor" in claims 1 (lines 5-6), and 3 (lines 5-6); the phrase "a larger emitter area than the first pnp transistor" in claims 4 (lines 10-11) and 7 (lines 10-11); and the phrase "a larger emitter area than the first npn transistor" in claims 5 (lines 10-11) and 8 (lines 10-11) are confusing. Nothing within the claims indicate if each of the first transistors have the same emitter area or not. Therefore, which first transistor does "the first...transistor" refer to within each of claims 1, 3-5, and 7-8? For example, is it the first transistor with the largest, or the smallest, emitter area, or does each second transistor have a larger emitter area than the total combined areas of the first bipolar transistors? Claim 4, lines 30-33 appear to be an incomplete thought. For example, how are the emitters and input terminals related with one another? It is suggested --is connected-- be added after "transistors" on each of lines 31 and 32 to make the limitations meaningful. Similar to claim 4 above, claim 5, lines 28-31 also appear to be an incomplete thought. For example, how are the collectors and input terminals related with one another? It is suggested --is connected-- be added after "transistors" on each of lines 30 and 31 to make the limitations meaningful. Claim 7, lines 25-26 has no clear relationship between the emitter and the input terminal. Therefore, it is suggested --is connected-- be added after "transistors" on line 26 to clarify the recited limitation. It is not clear how "a current source" of claim 9 (line 9) relates to

the "current sources" recited within claims 4 (line 19) or 5 (line 18). Similarly, it is not clear how "a current source" on line 5 of each of claims 10 and 11 relates to the "current sources" of claim 7 (line 16) or "a current source" of claim 8 (line 17). The use of "first npn transistor" (lines 3, 10-11, 14, 16, 19, 23-24, 27), "group of first npn transistors" (lines 7, 21-22, 25, 26, 28-29), "first npn transistors" (line 8), "second npn transistor" (lines 4, 15, 18, 20, 34), "group of second npn transistors" (lines 8-9, 31-32, 35, 36, and 39), and "second npn transistors" (lines 9 and 37) in claim 11 are confusing. It is suggested the transistors be more clearly identified with labels that distinguish between the various first/second npn transistors. Related to the above problem, it is not clearly understood how "a group of first npn transistors", "first npn transistors", "a group of second npn transistors", and "second transistors" in claim 11 (lines 7-9) relate to "a group of first npn transistors", "first npn transistors", "a group of second npn transistors", and "second npn transistors" already recited within claim 8 (lines 2, 3, 9, and 9-10, respectively). For example, what actually distinguishes the groups (and the npn transistors) of claim 11 from the groups (and the npn transistors) of claim 8?

Claim 4 recites the limitation "the corresponding power source" in lines 26-27. There is insufficient antecedent basis for this limitation in the claim.

Each of claims 6 and 9 recites the limitation "said differential voltage generating means" in lines 2-3 with insufficient antecedent basis for this limitation in each claim.

Claim 7 recites the limitation "the corresponding power source" in lines 23-24. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a

gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: How do the first and second input terminals of the differential pair of claim 10 relate to first/second input terminals of the current control means recited within each of claims 7 and 8?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

In so far as being understood, claims 1-3, and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by the applicant's own Prior Art (Fig. 5 or 6). Fig. 6 shows a constant voltage generating circuit (e.g. as disclosed on page 4, lines 6-7) comprising a group of first bipolar transistors NP21-NP2n including n first bipolar transistors NP21-NP2n; a group of second bipolar transistors NP11-NP1n including n second bipolar transistors NP11-NP1n, each having a larger emitter area than any one of the first bipolar transistors NP21-NP2n (e.g. each second bipolar transistor has an emitter area N times the emitter area of each first bipolar transistor); differential voltage generating means OP1 generates a differential voltage (applied to the gates of P1 and P2) effectively corresponding to a voltage equal to the sum of base emitter voltages of the n first bipolar transistors NP21-NP2n and a sum of the base emitter voltages of the n second bipolar transistors NP11-NP1n; and voltage amplification adding means P1,P2,R1,R2 amplifies

the differential voltage and adds the amplified voltage to the base emitter voltage of NP1n, one of the second bipolar transistors, to output constant voltage VOUT independent of temperature. [Note: the sum of the base emitter voltages of NP11-NP1n is found at the collector of NP1n, wherein the added voltage to that sum corresponds to the voltage drop across resistor R1.] This anticipates claim 1. Differential voltage generating means OP1 includes differential amplifier OP1. One of ordinary skill in the art understands that a differential amplifier has its own inherent offset voltage, and an input equivalent with a primary temperature characteristic (e.g. at a normal operating temperature). Therefore, claim 2 is also anticipated. Since claim 3 corresponds to the limitations recited within claim 2, which depends on claim 1, claim 3 is anticipated for the same reasoning as applied to claims 1-2 described above. The applicant's own Prior Art Fig. 5 shows a constant voltage generating circuit comprising a group of first pnp transistors PN21-PN2n including n first pnp transistors PN21-PN2n, a collector of each being grounded, a base of the first (PN21) of the first pnp transistors being grounded, a base of the k-th being connected to an emitter of a (k-1)-th of the first pnp transistors; a group of second pnp transistors PN11-PN1n including n second pnp transistors PN11-PN1n each having a larger emitter area (i.e. N times) the emitter area of any one of the first pnp transistors, a collector of each second pnp transistor being grounded, a base of a first (PN11) of the second pnp transistors being grounded, and a base of the k-th being connected to an emitter of the (k-1)-th of the second pnp transistors; current sources P11, P12, P2n, P22, and P21 connected to respective emitters of second pnp transistors PN11, PN12, and first pnp transistors PN2n, PN22, and PN21; the n-th (PN1n) of the group of second pnp transistors is coupled to its corresponding current source P1n through series coupled resistors R2,R1; current control means OP1 has first input terminal "-" of

differential amplifier OP1 connected to the emitter of the n-th (PN2n) transistor of the first pnp transistors, and second input terminal "+" of differential amplifier OP1 connected to the connection point between the two resistors R1,R2. Current control means OP1 controls the currents of the current sources by outputting a control signal. Due to the feedback connections of OP1, one of ordinary skill in the art would understand the potentials at the first and second input terminals would be the same. Also, since each differential amplifier is understood to have its own inherent offset voltage, and an input equivalent having a primary temperature characteristic as previously described, claim 7 is anticipated. Referring back to the applicant's own Prior Art Fig. 6, the constant voltage generating circuit comprises a group of first npn transistors NP21-NP2n including n first npn transistors NP21-NP2n, a base and collector of each being connected together, an emitter of first NP21 being grounded, and an emitter of a k-th first npn transistor being connected to the collector of a (k-1)-th of the first npn transistors; a group of second npn transistors NP11-NP1n including n second npn transistors NP11-NP1n, a base and collector of each being connected together, an emitter of first NP11 being grounded, and an emitter of a k-th second npn transistor being connected to the collector of a (k-1)-th of the second npn transistors; current source P1,P2, connected to the collector of the n-th transistor (NP2n) of the first npn transistors, supplies current to each of the groups, wherein two resistors R1,R2 are connected in series between current source P1,P2 and n-th NP1n of the second npn transistor; and current control means OP1 comprises first input terminal "-" of differential amplifier OP1 connected to the n-th transistor (NP2n) of the first npn transistors, and a second input terminal "+" of differential amplifier connected to the connection point between series connected resistors R1,R2. Due to the feedback connections of OP1, one of ordinary skill in the art would

understand the potentials at the first and second input terminals would be the same. Also, since each differential amplifier has its own inherent offset voltage, and an input equivalent having a primary temperature characteristic as previously described, claim 8 is anticipated.

In so far as being understood, claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Coady. Fig. 3 shows a constant voltage generating circuit (e.g. a bandgap voltage generator) comprising a group of first bipolar transistors Q1-Q2 including n first bipolar transistors Q1-Q2; a group of second bipolar transistors Q3-Q4 including n second bipolar transistors Q3-Q4 each having an emitter area n times larger than any one of the first bipolar transistors Q1-Q2; differential voltage generating means Q5-Q7,R10-R12,A1 generates differential voltage VBG effectively corresponding to a voltage equal to the sum of base emitter voltages of the n first bipolar transistors Q1-Q2 and a sum of the base emitter voltages of the n second bipolar transistors Q3-Q4; and voltage amplification adding means R1-R3 that effectively amplifies the differential voltage and adds the amplified voltage to the base emitter voltage of Q4, one of the second bipolar transistors, to output constant voltage VBG independent of temperature. [Note: the base emitter voltages of Q3-Q4 are summed at the collector of Q3, wherein the added voltage corresponds to the voltage drop across resistor R1.] This anticipates claim 1. Differential voltage generating means Q5-Q7,R10-R12,A1 includes differential amplifier (e.g. Q5-Q7,R10-R12, or A1, or Q5-Q7,R10-R12,A1), and one of ordinary skill in the art understands each differential amplifier has its own inherent offset voltage, and an input equivalent with a primary temperature characteristic (e.g. at a normal operating temperature), thus anticipating claim 2. Since claim 3 corresponds to the limitations recited within claim 2,

which depends on claim 1, claim 3 is also anticipated for the same reasoning as applied to claims 1-2 described above.

Allowable Subject Matter

Claims 4 and 5 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no motivation to modify or combine any prior art reference to ensure the constant voltage generating circuit includes the specific relationships between the two resistors, the first of the group of second pnp transistors, and the second of the group of second pnp transistors (e.g. see R1, R2, PN11, and PN12 of the applicant's own Fig. 1 (corresponding to the claim 4 limitations) or Fig. 3 (corresponding to the claim 5 limitations)).

Also, claims 6 and 9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Each of claims 6 and 9 depend on "claim 4 or 5", which have allowable subject matter as described above.

Claims 10 and 11 would also be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference to ensure the first/second npn transistors of the differential pair have different emitter areas, wherein it is believed the first/second input terminals of the differential pair are coupled to the first/second input terminals, respectively of the current control means (see claims 7 and 8).

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Fig. 2 of Greaves shows a constant voltage generating circuit comprising a group of first pnp transistors 99,98; a group of second pnp transistors 68,69; current sources 91-94,61-64 providing current to the emitters of their respective pnp transistors; current control means 43-48 for controlling the current; and resistor 65 coupled to the emitter of first pnp 68 of the second pnp transistors, as well as to the base of second pnp 69 of the second pnp transistors. However, there is no strong motivation to add a second resistor in series with resistor 65, wherein the connection point of the series resistors would be coupled to the base of 69. Sundby shows a constant voltage generating circuit in Fig. 3A comprising a group of first pnp transistors (not labeled, but shown on the left side of the figure); a group of second pnp transistors (not labeled, but shown on the right side of the figure); current sources (the four MOS transistors) providing current to the emitters of their respective pnp transistors; current control means (the unlabeled differential amplifier) for controlling the current; and series coupled resistors R1,R2. However, there is no strong motivation to move the series coupled resistors to be coupled to the first pnp transistor within the second pnp transistor group, wherein the connection point of the series resistors would be coupled to the base of the second pnp transistor within the group of second pnp transistors.

Note: Although the reference of Coady, used in formal rejections of claims 1-3 described previously, shows a differential amplifier with first/second bipolar transistors having different emitter areas (e.g. Q5 has area A, and Q6 has area nA), there is no strong motivation to modify or combine any prior art reference(s) to ensure a differential amplifier, within the current control

means as recited within each of claims 7 and 8, has a second npn transistor with a larger emitter area than the first npn transistor as recited within each of claims 10 and 11. It is also noted that Fig. 4 of Coady shows a differential amplifier with a differential pair of first/second npn first input transistors Q10/Q11 that have different emitter areas from one another, and first/second groups of second npn transistors Q12/Q13 coupled to the emitter of their respective first input transistors.

The prior art references cited on the IDS submitted Apr 1, 2004 were reviewed and considered. Although not used in any formal rejections described above, several of the references could have been used with respect to at least claims 1-3: 1) Fig. 2 of Chen et al. closely corresponds to the applicant's own Prior Art Fig. 5. Chen's circuit shows first/second groups of first/second bipolar transistors Q148,Q147,Q134/Q143,Q142,Q135; a differential voltage generating means OPAMP; and a voltage amplification adding means (e.g. P195,R137). 2) Fig. 1 of Japanese document 8-04449 shows a constant voltage generating circuit comprising first/second groups of first/second bipolar transistors 11/12 (with each transistor within 12 shown having an area of Xn); differential voltage generating means OPAMP 14; and voltage amplification adding means Q11,R1-R2, wherein the voltage dropped across the resistors is effectively added to the base emitter voltage drops of 13 to provide constant voltage VO. Of the other three references cited: A) Fig. 5 of Holle shows the connection point of series resistors R14,R13 being coupled to the base of first transistor Q12c of second group Q12a-Q12c, instead of to second transistor Q12b as recited within some claims. Also, the first and second groups of transistors within Holle's Fig. 5 circuit do not have the same number of transistors as understood from the claimed limitations, and the applicant's disclosure/figures. B) Japanese document 6-

043956 does not clearly show two groups of bipolar transistors, wherein the emitter area of the second group's transistors is larger than the first group's transistors. C) Fig. 1 of the PCT reference shows first group 32 with area a; second group 30 with area 8a; differential M1-M5,M14; and voltage amplification means/current sources M6-M13. However, this reference does not clearly show how the amplified voltage is added to the base emitter of one of the second group's transistors.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund
2 March 2005

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